WHAT IS CLAIMED IS:

1. A method for determining valid bytes in an m-byte
word accessed from a burst memory, comprising:

    receiving a plurality of access parameters; and

    generating an m-bit enable word from the access
parameters and a value of m, said m-bit enable word including
at least one valid bit corresponding to at least one valid
byte in the m-byte word.

2. The method of claim 1 further comprising making a
client request to memory, wherein the access parameters
include:

    a first address; and

    a byte count value indicating a number of bytes in
said client request to memory.

3. The method of claim 2, wherein generating the m-bit
enable word comprises:

    truncating a portion of the first address to produce
an n-bit word;

    generating an enable value from the n-bit word, the
byte count value, and the m value;

    generating an m-bit pre-shifted enable word from the
enable value and the m value; and

9   shifting the bits in the m-bit pre-shifted enable

10   word by a value of the n-bit word.

1   4.   The method of claim 3, wherein the n value equals a

2   base two logarithm of the m value minus one, and said n-bit

3   word comprises a plurality of bits between and including a

4   least significant bit and a bit in position n in the first

5   address.

1   5.   The method of claim 3, further comprising:

2   in response to the byte count value and the enable

3   value, determining whether an access to memory satisfies a

4   client request which generated the access.

1   6.   The method of claim 3, further comprising:

2   generating a second address for a subsequent access

3   to memory from the first address and the enable value.

1   7.   The method of claim 1, wherein the value of m is

2   thirty-two.

1   8.   A memory controller comprising:

2   a data input to receive a plurality of access

3   parameters from a client device and an access bytes value

4   indicating a number of bytes in a burst word from a memory

5   device; and

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6   an enable circuit to determine at least one valid

7   byte in the burst word in response to the plurality of access

8   parameters and the access bytes value.

1   9.   The memory controller of claim 8, wherein the

2   plurality of access parameters include:

3   a first address; and

4   a byte count value indicating a number of bytes in a

5   client request to memory.

1   10.   The memory controller of claim 9, further

2   comprising:

3   an enable word generator to generate an enable word

4   including at least one valid bit corresponding to the at least

5   one valid byte in the burst word.

1   11.   The memory controller of claim 10, wherein the burst

2   word comprises an m-byte word and the enable word comprises an

3   m-bit word.

1   12.   A system comprising:

2   a memory device comprising a plurality of memory

3   elements, each memory element having an associated address;

4   a client device;

5   a bus to pass data between the memory device and the

6   client device; and

7   a memory controller to control an access by the

8   client device to an m-byte burst word in the memory device

9   over the bus, said memory controller operating to receive a

10   plurality of access parameters from the client device and

11   determine at least one valid byte in the m-byte word in

12   response to the plurality of access parameters and a value of

13   m.

1   13.   The system of claim 12, wherein the memory

2   controller comprises an enable word generator to generate an

3   enable word including at least one valid bit corresponding to

4   the at least one valid byte in the burst word.

1   14.   The system of claim 12, wherein the memory

2   controller is operative to receive a client request to memory,

3   and wherein the plurality of parameters include:

4   a first address; and

5   a byte count value indicating a number of bytes

6   in said client request to memory.

1   15.   The system of claim 14, wherein the memory

2   controller is operative to determine a second address for a

3   subsequent access for the plurality of access parameters.

1   16. The system of claim 15, wherein the client is

2   operative to store the second address.

1   17. The system of claim 12, wherein the memory device is

2   a burst memory device.

1   18. The system of claim 12, wherein the memory

2   controller is operative to determine whether the access is a

3   last access required to satisfy a client request.

1   19. The system of claim 12, wherein the bus comprises a

2   read bus and a write bus.

1   20. Apparatus, including instructions residing on a

2   machine-readable medium, for determining valid bytes in an m-

3   byte word accessed from a burst memory, said instructions

4   causing the machine to:

5   receive a plurality of access parameters; and

6   generate an m-bit enable word from the access

7   parameters and the m value, said m-bit enable word including

8   at least one valid bit corresponding to at least one valid

9   byte in the m-byte word.

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1   21.   The apparatus of claim 20, wherein the access

2   parameters include:

3   a first address; and

4   a byte count value indicating a number of bytes in a

5   client request to memory.

1   22.   The apparatus of claim 21, wherein the instructions

2   to generate the m-bit enable word comprise instructions

3   causing the machine to:

4   truncate a portion of the first address to produce

5   an n-bit word;

6   generate an enable value from the n-bit word, the

7   byte count value, and the m value;

8   generate an m-bit pre-shifted enable word from the

9   enable value and the m value; and

10   shift the bits in the m-bit pre-shifted enable word

11   by a value of the n-bit word.

1   23.   The apparatus of claim 22, wherein the n value

2   equals a base two logarithm of the m value minus one, and said

3   n-bit word comprises a plurality of bits between and including

4   a least significant bit and a bit in position n in the first

5   address.

1   24.   The apparatus of claim 22, further comprising

2 instructions that cause the machine to:

3   determine whether an access to memory satisfies a

4 client request in response to the byte count value and the

5 enable value.

1   25.   The apparatus of claim 22, further comprising

2 instructions that cause the machine to:

3   generate a second address for a subsequent access to

4 memory from the first address and the enable value.

1   26.   The apparatus of claim 20, wherein the value of m is

2 thirty-two.